SYSTEMS AND METHODS FOR PROGRAMMING A SECURED CPLD ON-THE-FLY

ABSTRACT

On-the-fly reconfiguration of a secured CPLD. In one embodiment, a CPLD includes a novel security circuit that provides two different security control signals: an EEPROM/SRAM security signal and an EEPROM security override signal. The EEPROM/SRAM security signal prevents reading from both the EEPROM and the SRAM, and also prevents writing to the EEPROM. The EEPROM security override signal enables reading and writing for the EEPROM even when otherwise disabled by the EEPROM/SRAM security signal, but is active only when a specific set of conditions are met. These conditions can include, for example, the application of a sufficiently long erase pulse to the EEPROM array. Thus, the security on the EEPROM array is overridden only after the configuration data set stored in the EEPROM array has been erased. Reading from the SRAM is not enabled by the EEPROM security override signal. Therefore, the configuration data set is not compromised.